UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,517	02/04/2005	Taro Kamiko	2004 LW 2488 US	1666

48154 7590 03/28/2007

SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
ALSIP, MICHAEL	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,517	KAMIKO ET AL.	
	Examiner	Art Unit	
	Michael Alsip	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/04/2005, 11/14/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 15** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Consider **claim 15**, the applicant states that the second external memory is coupled to the system bus without an interface, the examiner does not understand how a device can be coupled to a bus without some kind of interface connecting the two.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 3-6, 8-13** are rejected under 35 U.S.C. 102(b) as being anticipated by Merrel et al. (US 5,829,038).

6. Consider **claim 1**, Merrel et al. discloses a data processing system having: at least one processor chip including a processor unit and an internal data cache (Col. 2 lines 59-65), and an interface which receives data to be written from the processor chip (where the cache hierarchy interfaces the main memory with the CPU and receives data to be written from the processor chip), the interface discarding the data received from

the processor chip (Col. 3 lines 46-67 and Col. 4 lines 1-37 where data written back to the cache hierarchy will eventually become a victim line and be evicted (discarded)).

7. Consider **claim 3**, as applied to **claim 1** above, Merrel et al. discloses a data processing system according to **claim 1** further including one or more further processing chips which have read/write access to external memory (Col. 2 lines 16-17, Col. 5 lines 22-26).

8. Consider **claim 4**, Merrel et al. discloses a method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting write instructions out of the integrated circuit (Col. 2 lines 60-65, Col. 3 lines 25-34), the method including discarding the write instructions (Col. 3 lines 46-67 and Col. 4 lines 1-37, where the write back instructions are canceled (discarded) if in the cache hierarchy there exists associated cache line in a lower level cache is modified or clean) and arranging for the program code operated by the processor to require only the data cache as memory (The purpose of the cache and control of the cache (replacement policy) is to reduce the amount of times the processor needs to access slower memory to retrieve its desired data by keeping as much of the require program data as possible in the cache, therefore if the program being run is only as big as the cache the program will use only the cache as its memory).

9. Consider **claim 5**, as applied to **claim 1** above, Merrel et al. discloses a data processing system according to **claim 1**, wherein the at least one processor chip comprises exactly one processor chip (Fig. 1).

10. Consider **claim 6**, as applied to **claim 1** above, Merrel et al. discloses a data processing system according to **claim 1**, wherein the at least one processor chip comprises two processor chips (Col. 2 lines 16-17, Col. 5 lines 22-264).

11. Consider **claim 8**, Merrel et al. discloses a data processing system comprising: a processor chip including an internal processor coupled to an internal data cache (Col. 2 lines 59-65); an external memory (Fig. 1); and an interface coupled between the processor chip and the external memory, the interface configured to receive memory data from the external memory and transfer the memory data to the processor chip (where the cache hierarchy interfaces the main memory with the CPU, transferring data to and from the main memory and CPU), the interface further configured to receive processor data from the processor chip and discard the processor data (Col. 3 lines 46-67 and Col. 4 lines 1-37 where data written back to the cache hierarchy will eventually become a victim line and be evicted (discarded)).

12. Consider **claim 9**, as applied to **claim 8** above, Merrel et al. discloses a data processing system according to **claim 8**, further comprising a control circuit coupled to the interface circuit, the control circuit providing a control signal to indicate whether data received by the interface should be discarded (the cache controllers for each cache in the hierarchy are the control circuits which contain the algorithms for determining which data is moved in and out of cache (cache replacement policy), including the eviction (discarding) of data in the cache).

13. Consider **claim 11**, as applied to **claim 8** above, Merrel et al. discloses a data processing system according to **claim 8**, further comprising: a second processor chip

that includes an internal processor coupled to an internal cache; and a second interface, wherein the second processor chip is coupled to the external memory through the second interface (Fig. 1, Col. 2 lines 16-17, Col. 5 lines 22-26, where each processor in the multi-processor cluster will have the same configuration as in fig. 1).

14. Consider **claim 12**, as applied to **claim 11** above, Merrel et al. discloses a data processing system according to **claim 11**, further comprising a system bus coupled to the processor chip, the second processor chip, the interface, and the second interface (Fig. 1, Col. 2 lines 16-17, Col. 3 lines 24-34, Col. 5 lines 22-26, wherein in a cluster the databus will be used in the same fashion as per the embodiment described).

15. Consider **claim 13**, as applied to **claim 12** above, Merrel et al. discloses a data processing system according to **claim 12**, further comprising a third processor chip coupled to the system bus (Fig. 1, Col. 2 lines 16-17, Col. 5 lines 22-26).

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

18. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel et al. (US 5,829,038) as applied to claim 1 above, and further in view of Klein (6,401,199 B1).

19. Consider **claim 2**, as applied to **claim 1** above, Merrel et al. discloses a data processing system according to **claim 1** in which the interface is coupled to a memory (Merrel et al: Col. 2 lines 59-65), but Merrel does not explicitly state that the interface passing data to the processor chip during initialization, whereas Klein does teach this (Klein: Col. 1 lines 22-63).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the processor chip initialize through the cache hierarchy interface of Merrel, because Klein teaches that running the bootstrap programs from RAM instead of ROM is faster (Klein: Col. 1 lines 54-63).

20. **Claims 7 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel et al. (US 5,829,038) as applied to **claims 1 and 9** above, and further in view of The Cache Memory book by Him Handy (Handy).

21. Consider **claims 7**, as applied to **claim 1** above, Merrel et al. discloses a data processing system according to **claim 1**, but does not explicitly disclose wherein the processor chip further includes an internal cache controller coupled between the internal data cache and the processor unit whereas Handy does teach this feature (Handy: Fig. 2.4 pages 42-49, all CPU/cache interactions are controlled by the cache controller which must intercept all of the CPU's signals).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have the cache controller between the internal data cache and processor unit in the system of Merrel et al., because Handy teaches that all CPU/cache interactions are controlled by the cache controller which must intercept all of the CPU's signals, therefore it would be obvious for the cache controller to be between the internal data cache and processor unit (Handy: Fig. 2.4 pages 42-49).

22. Consider **claim 10**, as applied to **claim 9** above, Merrel et al. discloses a data processing system according to **claim 9**, but does not explicitly state wherein the control circuit comprises a decoder (Handy: Fig. 5.5, pages 196-197).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a decoder in the control circuit in the system of Merrel et al., because Handy teaches that using a decoder with the control circuit for the cache reduces delays in determining cache hits and misses (page 196-197).

23. **Claims 14 and 15** are rejected under 35 U.S.C. 103(a) as being unpatentable over Merrel et al. (US 5,829,038) as applied to **claim 13** above, and further in view of Stewart et al. (US 5,157,780).

24. Consider **claim 14**, as applied to **claim 13** above, Merrel et al. discloses a data processing system according to **claim 13**, but does not explicitly state the system of claim 13 wherein the third processor chip comprises a master processing unit and wherein the processor chip and the second processor chip comprise slave processing units, whereas Stewart et al. does teach this feature (Fig. 1, Col. 1 lines 13-18).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a plurality of processors implemented in a master/slave configuration in the system of Merrel et al., because Stewart et al. teaches that it is common to use redundant processors to provide a fail-safe mode of operation (Col. 1 lines 13-18).

25. Consider **claim 15**, as applied to **claim 14** above, Merrel et al. discloses a data processing system according to **claim 14**, further comprising a second external memory coupled to the system bus without an interface coupled between the second external memory and the system bus (The examiner is taking official notice to the fact that it is well-known and common in the art to have a volatile main memory to receive its data from a secondary non-volatile memory (hard drive) in computer systems).

It would have been obvious to one of ordinary skill in the art at the time of the invention to have a second external memory coupled to the system bus in the system of Merrel et al., because it is notoriously well-known and common in the art to have a hard disk supplying data to the volatile main memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Alsip whose telephone number is 571-270-1182. The examiner can normally be reached on Monday through Friday 7:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Michael Alsip
Examiner
Art Unit 2186

MA

March 13, 2007

PIERRE BATAILLE
PRIMARY EXAMINER
3/14/07